Remarks:

All claims have been rewritten to specify the invention's patentability over prior art, and to overcome the technical objections of the office action.

The Rejection of claim 1 on Suzuki is overcome.

The office action rejected this claim under 35 U.S.C. § 103(a) as being unpatentable in view of Suzuki et al (Japan Patent 11-145322). Claims 1 has been rewritten as claim 19 to define the patentability over the reference. Applicant requests reconsideration of this rejection, as now applicable to claim 19, for the following reasons:

1) Suzuki is lacking in features to meet claims.
2) There is no justification in Suzuki that the reference be modified in a manner to meet the claims.
3) The novel construction provides superior performance.

Summary of the Reference and Differences to the present Invention.
Suzuki describes a semiconductor package with a recess, where the package is formed from three components, a metal plate with a recess, an insulating substrate with circuitry, and an adhesive layer to bond the plate to the substrate. In the central part of the insulating substrates is a device hole. The device hole is for mounting the integrated circuit on the metal plate, as the means to remove heat from the integrated circuit. The device hole removes all circuitry of the insulating substrate under the die. Only one signal type or voltage is possible under the die, which is that assigned to the metal plate. Electrical connections to the metal plate are made by solder on through small holes on the periphery of package, and with wirebond from the die through the device hole. The spacing between the signal layers on the insulating substrate and the metal plate is defined by the thickness of the adhesive layer. This adhesive layer is attached at the same time as the solder for the peripheral electrical connections, a complicated process involving solder, flux, lamination over a 3 dimensional surface.

The present invention differs from Suzuki by allowing multiple signal types and voltages, in the total recess area, including the slopped sides of the recess, and under the die. The electrical connections between the substrate and the integral metal plate are made by copper. There is no limitation on the location of these electrical contacts, and the electrical contacts in the central area are not made by wirebonds. The spacing between the signal layers and the integral metal plate is defined by a the lamination step, a well controlled printed wiring board fabrication technique, and does not involve the additional materials of solder and flux.

Suzuki is lacking in features to meet claims.
The structure and claims in Suzuki are dependent on a device hole in the insulated substrate. The device hole is to allow the die to be mounted to the metal plate, and therefore provide a means to remove heat. The device hole removes the possibility of complex circuitry under and around the die, and limits the signal types under the die to a single voltage.

Applicant has refined claim 19, and now includes ability to have complex circuitry in the recess, including under the die. There are also included metallic vias in the printed wiring board on the die to conduct heat from the die. Applicant submit the rejections to the claim are overcome and should be withdrawn.

Suzuki lacks justification that the reference be modified in a manner to meet the claims.

There is no suggestion in Suzuki that the reference be modified to allow circuitry under the die. The need to have a device hole, in fact, teaches away from and suggests the opposite of providing circuitry under the die.

Applicant submits that there is an improvement over Suzuki, that is not suggested in prior art, and the applicant submits the rejections should be withdrawn.

The novel construction provides superior performance.

Although Suzuki and the present invention are similar in structure, the present invention has superior function and performance over Suzuki. In semiconductor packaging, the electrical performance is a critical criteria for the successful adoption of a new technology. The fabrication steps and materials often limit the electrical properties, the distribution of the electrical properties and the magnitude of unwanted parasitic values. Examples of improved electrical properties follow:

Characteristic Impedance The characteristic impedance of a signal trace is dependent on the thickness of the dielectric layer between the signal trace an the reference plane. In Suzuki, the process for dielectric layer is done at the same time as electrical connections are made to the metal plate, using solder and flux. This is a complex process, and requires controlling multiple variables for laminating the adhesive and reflowing the solder, which will result in a larger variability in the thickness of the dielectric layer, and therefore a larger variation in characteristic impedance of a signal trace due to the added complexity of process in Suzuki compared to the present invention. This larger variation from the construction of Suzuki reduces the signal integrity, that can be achieved with consgtruction of the present invention.
Noise Isolation The signal return layer of a bus with a large number of signals is noisy, and designs often isolate the ground return plane of a noisy bus from the ground voltage of the

core logic in the integrated circuit. In Suzuki, the metal plate is both connected to the backside of the die and acts as the signal return plane. As the backside of the die is normally the same as the ground voltage of the core logic, then in Suzuki it is not possible to isolate the signal return noise from the ground voltage of the core logic. In the present invention patterning under the die allows isolation of the backside of the die from the metal plate, allowing the metal plate to be used as the ground return plane of a noisy bus of signals.
Parasitic inductance In Suzuki the contact from the metal plate to the die is made with a wirebond, which has a separate path from the wires of a signal. This separation of paths adds a parasitic inductance to the signal trace, reducing the frequency bandwidth. In the present invention with circuitry throughout the recess the wires can be shorter and can follow the same path, reducing the parasitic inductance over Suzuki.
RF filters For high frequency RF signals, it is desirable to place filter circuits close to the bond pads of the integrated circuit. The region around the die is normally congested with bond pads and the fanout from bond pads. It would be advantage to use the area under the die to place the filter circuits. In Suzuki this is not possible, while present invention allows for filter circuits to be designed under the die.
Die backside bias One method to reduce leakage currents in a submicron integrated circuits is to provide a voltage to the backside of the die that is slightly lower than ground voltage of the core logic. This is not possible in Suzuki, unless the metal plate is use to supply the voltage to bias the backside of the die, in which can it is not available to be used as the signal ground return plane. In the present invention circuitry under the die can be use to isolate and bring voltage to the backside of the die, separate from the metal plate, allowing the metal plate to be used as a ground return.

Applicant submits there is a synergistic affect from the construction of present invention, which provide superior electrical performance over Suzuki. Applicant submits this allows new and unexpected results, as an improvement over Suzuki, and request that the rejections should be withdrawn.

The Rejection of claim 4 on Suzuki is overcome.

The office action rejected this claims under 35 U.S.C. § 103(a) as being unpatentable in view of Suzuki et al (Japan Patent 11-145322). Claim 4 has been rewritten as claim 20 to define the patentability over the reference. Applicant requests reconsideration of this rejection, as now applicable to claim 20, for the following reason:

1) Suzuki is lacking in features to meet claims.
2) There is no justification in Suzuki that the reference be modified in a manner to meet the claims.

Suzuki is lacking in features to support claims.
Claim 4 connects the plurality of die bond pads to package bond pads with solder balls. In this configuration the package bond pads would need to be under the die. In Suzuki there is a device hole that removes all circuitry under the die, and therefore no possibility to have package bond pads under the die. There is no suggestion in Suzuki that the reference be modified to allow circuitry under the die. The need to have a device hole, in fact, teaches away from and suggests the opposite of providing circuitry under the die.

Applicant submits it is not possible under Suzuki to use solder balls to connect the die bond pads to the package pads. The applicant submits the rejection should be withdrawn.

Suzuki lacks justification that the reference be modified in a manner to meet the claims.
There is no suggestion in the reference for the use of solder balls to connect the die pads to the package bond pads.

Applicant submits that there is an improvement over Suzuki, that is not suggested in prior art, and the applicant submits the rejections should be withdrawn.

The Dependent Claims are Patentable Over Suzuki.

New dependent claims 21 to 29 incorporate all the subject matter of claim 19 and add additional subject matter which makes them independently patentable over the references.

Claim 20 defines the means to connect the die bond pads to the package bond pad with solder balls. This feature cannot be supported in Suzuki.

Claim 21 and 22 restrict the features of the printed wiring board to provide circuitry under the die, a feature that is missing in Suzuki

Claims 23 to 28 define the characteristics of the metal core of the printed wiring board. Suzuki and Nishihara reference the same materials, but when combined with Suzuki do not constitute a structure with all the features of the present invention.

Claim 29 provides for the additional feature of solder balls on the package bond pads. Suzuki includes this features, but on a structure which does not contain all the features of the present invention.

Claim 30 and 31 describe a method to fabricate the structure of claim 19.

Conclusion

For all the above reasons, the applicant submits that the specification and claims are now in order, and that the claims are patentable over the prior art. Therefore the applicant submits this applications is now acceptable for allowance.

Conditional Request For Constructive Assistance

The applicant has amended the specifications and claims of this application to define novel structure, which is also not obvious. If for any reason this application is not in condition for full allowance, the applicant respectively request the assistance of the Examiner for suggestions to make any necessary changes such that the application is in an allowable condition.

Respectfully,

Applicant: Thomas J. Massingill 4/3/2006

Thomas J. Massingill

Thomas Massingill
170 Northridge Drive
Scotts Valley, CA 95066
408-482-8382

Certificate of Mailing

I certify that this correspondence will be deposited with the United States Postal Service as first class mail with proper postage affixed in an envelope addressed to: "Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450' on the date below.

Date: April 13, 2006 Thomas J. Massingill Applicant